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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,279	11/19/2003	Steven J. Koester	YOR920030533US1 (17110)	7401
23389 7590 03/13/2007 SCULLY SCOTT MURPHY & PRESSER, PC 400 GARDEN CITY PLAZA SUITE 300 GARDEN CITY, NY 11530			EXAMINER MAI, ANH D	
			ART UNIT	PAPER NUMBER
			2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/13/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/717,279	KOESTER, STEVEN J.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 December 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,2 and 4-21 is/are pending in the application.
- 4a) Of the above claim(s) 10-21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 4-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Status of the Claims*

1. The Amendment filed December 26, 2006 is acknowledged. Claims 1, 2 and 4-9, as filed on June 26, 2006 are resubmitted. Non-elected invention, claims 10-21 have been withdrawn. Claims 1, 2 and 4-21 are pending.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 4 and 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Xiang (U.S. Patent No. 6,749,527) as previously applied.

With respect to claim 1, Xiang teaches a semiconductor field-effect transistor device as claimed including:

a first strained layer (42) of semiconductor material doped of a first dopant type formed on a substrate (40);

a source region and a drain region (64) implanted with dopants of a second opposite type;

a gate electrode (54) separated from the first layer (42) by a dielectric region (56), and positioned between the source and drain regions (64);

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substrate (40) inherently having one or more dislocation or crystal defects that extends continuously from the source region to the drain region (64) at the interface between the first strained layer (42) of semiconductor material and substrate (40), and

blocking impurity dopant materials that partially or fully occupies each one or more dislocation or crystal defects, wherein the blocking impurity dopant materials substantially inhibit diffusion of the implanted source and drain dopants from diffusing along the dislocations or crystal defect (185). (See Fig. 3i).

With respect to claim 2, the first strained layer (42) of semiconductor material of Xiang comprises material selected from the group comprising Si.

With respect to claim 4, the semiconductor substrate (40) of Xiang includes a SiGe relaxed substrate.

With respect to claim 7, the blocking impurity of Xiang is a neutral-type impurity.

With respect to claim 8, the blocking impurity of Xiang is a group IV impurity.

With respect to claim 9, the blocking impurity of Xiang is C.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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3. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang '527 as applied to claim 1 above, and further in view of Noda et al. (U.S. Patent No. 6,432,802), of record, as previously applied.

Xiang teaches that halo region are doped with dopant of opposite the conductivity to the source and drain regions are formed.

Thus, Xiang is shown to teach all the features of the claim with the exception of explicitly disclosing the specific impurity for the halo region.

However, Noda teaches that it is well known in the art to form the halo region utilizing indium (In) for p-channel device and antimony (Sb) for n-channel device.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the halo blocking region of Xiang utilizing In or Sb blocking impurity as taught by Noda to prevent diffusion of the source/drain dopants into the channel region.

Note that, P, As or Sb as well as B or In, are well known in the art to be used for source/drain dopant in a p-channel or n-channel device, respectively.

#### ***Response to Arguments***

4. Applicant's arguments filed December 26, 2006 have been fully considered but they are not persuasive.

#### **Rejection under 35 U.S.C. 102:**

Applicant argues:

1) There is actually no teaching or suggestion in Xiang that one or more dislocation or crystal defects extend continuously from the source region to the drain region at an interface

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between said first strained layer of semiconductor material and said substrate.

However, the “crystal defects extend continuously from the source region to the drain region at an interface between first strained layer of semiconductor material and substrate” is inherent of growing strain layer on a substrate. This extension can be seen in the Description of the Prior Art, page 1, Fig. 1a, “These threading dislocations continue to extend to the sample surface after growth of the strained Si cap layer. During high-temperature processing, additional misfit dislocations can form if the *threading dislocations glide along the interface* of the relaxed SiGe layer and the strained Si layer”.

Clearly the dislocation does extend continuously from source region to drain region.

2) Moreover, Xiang *does not recognize nor makes mention* that, after a drain/source region annealing process, the misfit locations (sic) that extend continuously from the source region to the drain region provide a leakage path from the drain to the source....

However, the **inherent** present of the misfit dislocation along the interface as discussed above, does not required recognition or mention, since it is known among the one having ordinary skill in the art.

3) The present invention, addresses the process-induced dislocation leakage path problem whereby dopant atoms diffuse or segregate along the dislocations if the gate length is sufficiently short resulting in one or more of: poor turn-off behavior, high leakage in the subthreshold region ( $V_{gs} < 0$ ) and other dislocation-related failures.

However, the above argument is directed to the Applicant's study rather than the subject matter that inherently occurs in the reference to Xiang.

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4) The solution of the invention as claimed in Claim 1 is to provide blocking impurity dopant materials that partially or fully occupies each said one or more dislocation or crystal defects, such that the blocking impurity dopant materials substantially inhibit diffusion of said implanted source and drain dopants from diffusing along said dislocation or crystal defect as required by Claim 1 of the present invention.

5) Applicants find no teaching or suggestion in Xiang that the carbon atoms implanted into the active region of the strained Silicon layer of the MOS device partially or fully occupy each said one or more dislocation or crystal defects to substantially inhibit diffusion of implanted source and drain dopants from diffusing along the dislocation or crystal defect as required by Claim 1 of the present invention.

However, the effect of the heavy ions such as Sn into Si has been studied in C. Claeys et al., J. Electrochem. Soc. 148, G 738 (2001), and it is found that Sn acts as a vacancy getter.

These results therefore suggest that Sn may also acts as a getter for dislocations.

Applicant also recognizes that carbon is behaved similar to Sn for the same purpose.

Therefore, the present of carbon ions in the device of Xiang also inherently function as claimed.

6) Xiang actually teaches implanting carbon atoms into the active region of the strained Silicon layer of the MOS device for purposes of forming a silicon carbon alloy having a greater carrier mobility than that of an undoped Strained silicon layer (Xiang at paragraph bridging columns 4 and 5). That is, the MOS active device region is implanted with carbon atoms for purposes of raising the effective strain induced at the strained silicon layer than would be normally imparted by the concentration of Ge in the underlying SiGe layer. Xiang describes a concentration of about 1% carbon introduced into the strained silicon layer to effectively increase the strain (and hence, carrier mobility) of the strained silicon layer. As such, it can only be deduced that the carbon atom implantation in this layer are diffused throughout the strained layer to provide said enhanced mobility with the energy and dose of the implanted carbon selected to achieve the desired strain increase.

However, as discussed above, the heavy ions acts as getter for dislocation, which means the ions occupied the dislocation region. Therefore, beside what Xiang have found, increasing the strain, carbon also inherently function as claimed.

7) Thus, Xiang addresses a different problem than the problem addressed by the present invention....

Although addressing a different problem, the device of Xiang also inherently, implicitly solve the same problem as the present invention.

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8) Xiang's doping of carbon atoms in the strained Si layer is not suggestive that the implanted carbon atoms as provided in Xiang would inherently partially or fully occupy each said one or more dislocation or crystal defects to provide the same function as claimed in the present invention.

As discussed above, as a getter for dislocation, similar to Sn, carbon also occupies the dislocation, thus, the limitation "partially or fully occupy each said one or more dislocation or crystal defects" is anticipated.

For the reasons above, the claims are anticipated by Xiang, therefore, the rejections are maintained.

### ***Conclusion***

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.



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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



**ANH D. MAI**  
**PRIMARY EXAMINER**